FIG. **6** illustrates in more detail the correction of a second output signal **370**, based on a detected frequency error in the first output signal **350** and a predicted or detected error in second output signal **370**. If it is known that all or part of the detected frequency error in the first output signal **350** is caused by a reference frequency error, for instance, then a corresponding error can be predicted for the second output signal **370**. However, other sources may also contribute to a predicted error. In any case, at block **455**, frequency correction circuit **310** calculates an adjustment parameter based on the detected frequency error in first output signal **350** and the detected or predicted error in second output signal **370**. The predicted error may comprise, for example, an anticipated Doppler shift in a positioning signal received from a GPS receiver. The calculation of the adjustment parameter takes into account the error detected in the first output signal **350**, either directly, or by accounting for corrections made to the first output signal **350** via adjustments made to the frequency divider **220'** and/or reference clock **150**. For instance, frequency correction circuit **310** might in some embodiments correct the first output signal **350** by adjusting only the frequency-divide ratio in divider **220'**. In this case, frequency correction circuit **310** might calculate an adjustment parameter for use in correcting second output signal **370** based directly on the detected error. In another embodiment, at least a portion of the detected frequency error may be corrected in the first output signal **350** by adjusting reference clock **150**, in which case the allocation of error, along with the detected frequency error, may be used in calculating the desired adjustment to the second output signal **370**.

Those skilled in the art will appreciate, in view of the preceding discussion, the applicability of the methods and circuits described herein to a communications device, such as the multi-function communications device pictured in FIG. **1**. Communications device **100** comprises a communications transceiver circuit, pictured in FIG. **1** as a cellular transceiver circuit **110**, and a second receiver circuit, pictured in FIG. **1** as GPS receiver **120**. Frequency synthesizer circuit **140** may correspond to frequency synthesizer circuit **300**, pictured in FIG. **3**, and comprise first and second phase-locked loop circuits **200'** and **200"** configured to generate first and second output signals **350** and **370**, respectively, phase-locked to a common reference clock signal from reference clock **150**. The first output signal is used by the communications transceiver circuit **110** and the second output signal is used by the second receiver circuit **120**.

Frequency synthesizer circuit **140** may further comprise a frequency correction circuit **310**. The frequency correction circuit **310** is configured to correct the first output signal by adjusting a first frequency-division ratio in the first phase-locked loop circuit **200'** and generating a control signal to adjust the frequency of the reference clock signal, in response to a frequency error in the first output signal detected by the communications transceiver circuit **110**. In some embodiments, the frequency correction circuit **310** may be further configured to calculate an adjustment parameter based on the detected frequency error and the adjustment to the reference clock frequency, and to correct the second output signal by adjusting a second frequency-division ratio in the second phase-locked loop circuit **200"**, using the adjustment parameter. In some embodiments, frequency correction circuit **310** may be configured to schedule adjustments to any or all of the phase-locked loop circuits **200'** or **200"** or the reference clock **150**, to avoid frequency discontinuities during one or more satellite signal measurements made by the satellite positioning receiver circuit.

Those skilled in the art will appreciate that the foregoing description and the accompanying drawings represent non-limiting examples of the methods and apparatus taught herein for synthesizing multiple signals phase-locked to a common reference. Accordingly, the present invention is limited only by the following claims and their legal equivalents.

What is claimed is:

1. A frequency synthesizer circuit, comprising:

a first phase-locked loop circuit configured to generate a first output signal phase-locked to a reference clock signal;

a second phase-locked loop circuit configured to generate a second output signal phase-locked to the same reference clock signal; and

a frequency correction circuit configured to correct the first output signal by adjusting a first frequency-division ratio in the first phase-locked loop circuit and generating a control signal to adjust the frequency of the reference clock signal, in response to a detected frequency error in the first output signal.

2. The frequency synthesizer circuit of claim **1**, wherein the frequency correction circuit is configured to generate the control signal to correct for one or more relatively long-term sources for the detected frequency error and to determine the adjustment of the first frequency-division ratio to correct for one or more relatively short-term sources.

3. The frequency synthesizer circuit of claim **2**, wherein the frequency correction circuit is configured to determine the adjustment of the first frequency-division ratio based on a Doppler shift resulting from motion of the frequency synthesizer circuit relative to a remote transmitter.

4. The frequency synthesizer circuit of claim **2**, wherein the frequency correction circuit is configured to generate the control signal based on a reference frequency error in the reference clock signal.

5. The frequency synthesizer circuit of claim **2**, wherein the frequency correction circuit is configured to generate the control signal based on an average of the detected frequency error over an averaging interval and to determine the adjustment of the first frequency-division ratio based on the difference between the average and the detected frequency error.

6. The frequency synthesizer circuit of claim **1**, wherein the frequency correction circuit is further configured to calculate an adjustment parameter based on the detected frequency error and the adjustment to the reference clock frequency, and to correct the second output signal by adjusting a second frequency-division ratio in the second phase-locked loop circuit, using the adjustment parameter.

7. The frequency synthesizer circuit of claim **1**, wherein the frequency correction circuit is configured to schedule the adjustments of the reference clock signal frequency and the first frequency-division ratio to avoid frequency discontinuities in the first or second output signals, or both, during one or more application-dependent time intervals.

8. The frequency synthesizer circuit of claim **1**, wherein the frequency correction circuit is configured to apply successive adjustments to the reference clock signal frequency and the first frequency-division ratio to shift, over time, a greater proportion of the overall correction of the detected frequency error to the adjustments of the reference clock signal frequency.

9. A frequency synthesizer circuit, comprising:

a first phase-locked loop circuit configured to generate a first output signal phase-locked to a reference clock signal;